

PTC/SB/08A (10-01)
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE				Filing Date . Septer		ber 11, 2003	
STATEMENT BY APPLICANT				First Named Inv nt r	Jason H. Anderson		
STATEMENT DY APPLICANT				Art Unit	Unknown	2825	
(use as many sheets as necessary)			cessary)	Examiner Name	Unknown	siek .V.	
Sheet	1	of	1	Attorney Docket Number	X-1396 US		

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VS		HALTER, JONATHAN P., "A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuits," IEEE Custom Integrated Circuits Conference, 1997, pages 475-478, IEEE, 3 Park Avenue, 17th Floor, New York, NY., 10016-5997.			
US		YEAP, GARY, "Practical Low Power Digital VLSI Design," 1998, pages 59-72, available from Kluwer Academic Publishers, 101 Philip Drive, Assinippi Park, Norwell, Massachusetts, 02061			
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## **INFORMATION DISCLOSURE** STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet of

Complete If Known						
Application / Conf. No.	10/659,918 / 6014					
Filing Date	September 11, 2003					
First Named Inventor	Jason H. Anderson					
Art Unit	2858 2876					
Examiner Name	Unknown 5,eh					
Attorney Docket Number	X-1396 LIS					

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<b>1/&gt;</b>		ANDERSON, JASON H., "Active Leakage Power Optimization for FPGAs," FPGA '04, February 22-24, 2004, Monterey, California, USA, 9 pages, available from janders@eecg.toronto.edu or Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124			
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